Although the claims are not amended by this submission, this listing of claims is provided for ease of reference.

Listing of claims:

1. (Previously presented) A computer system comprising:

a driver interface including a plurality of output buffers;

a receiver interface coupled to the plurality of output buffers of said driver interface via interconnect, said interconnect comprising a plurality of traces of varying lengths; and

a programmable delay element coupled to said driver interface, said delay element being programmed to offset switching of said output buffers with respect to each other and to delay switching of said output buffers by a delay corresponding to a length of a trace coupled to a respective buffer.

2. (Original) The computer system of claim 1, wherein said delay is inversely proportional to said length.

3. (Original) The computer system of claim 1, wherein said delay is proportional to a difference between said length and a length of a longest trace.

4. (Original) The computer system of claim 1, wherein said receiver interface is wider than said driver interface.

5. (Original) The computer system of claim 1, wherein said driver interface is coupled to a memory controller, and said receiver interface is coupled to memory.

6. (Canceled)

7. (Original) The computer system of claim 1, wherein no delay is introduced in a signal connected to a longest trace.

8. (Previously presented) The computer system of claim 1, wherein said delay element includes a delay locked loop.

9. (Previously presented) A computer system comprising:

a plurality of output latches of a first interface;

interconnect coupling said output latches to a second interface and comprising a plurality of traces of varying lengths, said traces being configured to propagate signals from said output latches to said second interface;

a plurality of multiplexers, each multiplexer coupled between a latch of said output latches and a delay element comprising a plurality of variable delay outputs; and

a plurality of programmable registers, each register coupled to a multiplexer of said multiplexers, said registers being programmable to select one of said plurality of variable delay outputs to offset switching of said output latches with respect to each other and in accordance with a length of a trace that propagates a signal of said latch.

10. (Original) The computer system of claim 9, said plurality of variable delay outputs comprising a clock signal and phase-shifted versions of said clock signal.

11. (Original) The computer system of claim 9, wherein said first interface is coupled to a memory controller, and said second interface is coupled to memory.

12. (Previously presented) A method comprising:

connecting a first interface to a second interface with interconnect comprising traces configured to propagate signals, said traces having varying lengths; and

programming a delay element to offset switching of signals output by said first interface with respect to each other and to delay said signals output by said first interface for propagation to said second interface by a delay corresponding to respective lengths of traces propagating said output signals.

13. (Original) The method of claim 12, further comprising:

providing a plurality of variable delay outputs from said delay element; and

selecting one of said plurality in accordance with a length of a trace of said traces.

14. (Original) The method of claim 12, wherein said delay is inversely proportional to said respective lengths.

15. (Original) The method of claim 12, wherein said delay is proportional to a difference between said respective lengths and a length of a longest trace.

16. (Original) The method of claim 12, wherein said programming is performed by software.

17. (Original) The method of claim 16, wherein said software is a BIOS program.

18. (Previously presented) An interconnect for a computer system, comprising:

a plurality of traces, each having a respective length;

a plurality of programmable delay outputs, each provided on a ~~terminal~~ driver end of one of the traces, and characterized by a delay to offset switching, with respect to each other, of signals coupled to said plurality of traces, the delay corresponding to a difference between the length of the respective trace and the length of a longest trace.

19. (Original) The interconnect of claim 18, wherein no delay output is provided for the longest trace.

20. (Previously presented) A computer system comprising:

first and second agents; and

an interconnect coupled to the first and second agents and comprising:

a plurality of traces, each having a respective length; and

a plurality of delay outputs, each provided on a driver end of one of the traces, and characterized by a programmable delay to offset switching of outputs of one

of said first and second agents with respect to each other and corresponding to a difference between the length of the respective trace and the length of a longest trace.

21. (Previously presented) The computer system of claim 20, wherein a terminal end of a trace is at a receiver interface of either of said first and second agents.

22 - 25 (Canceled)

26. (Previously presented) A method comprising:

connecting a receiver interface to interconnect comprising traces configured to propagate signals, said traces having varying lengths;

providing a plurality of variable delay outputs from a delay element; and

programming said delay element to offset switching of outputs coupled to said interconnect and to delay signals from said outputs received at said receiver interface by a delay corresponding to respective lengths of traces propagating said received signals.

27. (Previously presented) The method of claim 26, further comprising:

selecting one of said plurality in accordance with a length of a trace of said traces.

28. (Original) The method of claim 26, wherein said delay is directly proportional to said respective lengths.

29. (Original) The method of claim 26, wherein said programming is performed by software.

30. (Original) The method of claim 29, wherein said software is a BIOS program.

31. (Previously presented) The computer system of claim 1, wherein the programmable delay element comprises:

a phase-shifting device to output a plurality of clock signals phase-shifted with respect to each other; and

a plurality of selection devices each coupled to the plurality of phase-shifted clock signals;

the selection devices being programmed to select from among the plurality of phase-shifted clock signals to effect said offset and delay.